REMARKS

At the outset, the Examiner is thanked for the thorough review and consideration of the pending application. The Non-Final Office Action dated August 10, 2004 has been received and its contents carefully reviewed.

Claims 1-20 are pending in the current application. Applicant withdraws claims 9 and 12-20 as a result of the election of Species A filed on May 21, 2004. Applicant adds new claims 21 and 22 dependent from claims 1 and 7, respectively. Claims 1-8, 10, 11, 21 and 22 are pending after this amendment.

The Examiner objects to claims 2 and 4. Applicants amend claims 2 and 4 to clarify the structure claimed therein. Accordingly, Applicants respectfully request the Examiner withdraw the objection to these claims.

In the Office Action, claims 1-4 and 6 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent 6,552,764 B2 to Fujioka et al (Fujioka '764). Claim 5 is rejected under 35 U.S.C. §103(a) as being unpatentable over Fujioka '764 in view of U.S. Patent 6,336,331 B1 to Sakamoto et al. Claims 7 and 8 are rejected under 35 U.S.C. §103(a) as being unpatentable over Fujioka '764 in view of U.S. Patent 6,400,439 B1 to Fujioka et al (Fujioka '439). Claim 10 is rejected under 35 U.S.C. §103(a) as being unpatentable over Fujioka '764. Claim 5 is rejected under 35 U.S.C. §103(a) as being unpatentable over Fujioka '764 in view of Japanese Patent Application 02-220032 to Obara et al.

Applicants amend claims 1, 7, and 10 to recite more clearly the features of the invention in the claims.

The rejection of claims 1-8, 10 and 11 is respectfully traversed and reconsideration is requested. Independent claim 1 is allowable over the cited references in that it recites a combination of elements including, for example, "a gate insulating layer on the lower substrate in the display area and a non-display area of the lower substrate;...a seal pattern of a constant

thickness formed on the gate insulating layer in a boundary region between the display area and the non-display area of the lower substrate".

None of the cited references including Fujioka '764, Fujioka '439, Sakamoto, and Obara, singly or in combination, teaches or suggests at least this feature of the claimed invention. The structure of claim 1 of the present invention is different from the structures in the cited references in that none of the references disclose "a gate insulating layer on the lower substrate in the display area and a non-display area of the lower substrate;...a seal pattern of a constant thickness formed on the gate insulating layer". The Examiner acknowledges that Fujioka '764 does not disclose or suggest that the seal pattern contacts the gate insulating layer (Office Action, page 7). However, Fujioka '439 also does not disclose or suggest this feature. Fig. 20 of Fujioka '439 clearly shoes that the sealing material 28 contacts both the insulating material 50 and the gate insulating layer 38 making the thickness of the sealing material variable.

Fujioka '439 discloses that "the sealing material 28 can be directly contacted with the gate insulating film 38 of the substrate 22 and the light-shading layer (a black matrix made from a metal such as Cr) of the substrate 24 in the adhesion reinforcing portion 50a" (Fujioka '439, column 18, lines 50-54). Therefore, Fujioka '439 does not disclose or suggest "a gate insulating layer on the lower substrate in the display area and a non-display area of the lower substrate;...a seal pattern of a constant thickness formed on the gate insulating layer" as recited in claim 1.

The Examiner implicitly acknowledges that none of Sakamoto, Obara or the other cited references disclose or suggest this feature. Accordingly, claim 1 and claims 2-6 and 21 which depend from claim 1 are allowable over the cited reference.

Independent claim 7 is allowable over the cited references in that it recites a combination of elements including, for example "forming a seal pattern in the boundary region between the display area and the non-display area of the lower substrate, the seal pattern having a constant thickness and contacting a gate insulating layer, said gate insulating layer on the lower substrate in the display area and a non-display area of the lower substrate".

The structure of claim 7 of the present invention is different from the structures in the cited references in that none of the references disclose "the seal pattern having a constant thickness and contacting a gate insulating layer, said gate insulating layer on the lower substrate in the display area and a non-display area of the lower substrate". The Examiner acknowledges that Fujioka '764 does not disclose or suggest that the seal pattern contacts the gate insulating layer (Office Action, page 7). However, as discussed above, Fujioka '439 also does not disclose or suggest this feature. Fig. 20 of Fujioka '439 clearly shoes that the sealing material 28 contacts both the insulating material 50 and the gate insulating layer 38 at different heights making the thickness of the sealing material variable.

Fujioka '439 discloses that "the sealing material 28 can be directly contacted with the gate insulating film 38 of the substrate 22 and the light-shading layer (a black matrix made from a metal such as Cr) of the substrate 24 in the adhesion reinforcing portion 50a" (Fujioka '439, column 18, lines 50-54). Therefore, Fujioka '439 does not disclose or suggest "the seal pattern having a constant thickness and contacting a gate insulating layer" as recited in claim 7.

The Examiner implicitly acknowledges that none of Sakamoto, Obara or the other cited references disclose or suggest this feature. Accordingly, claim 7 and claims 8 and 22 which depend from claim 7 are allowable over the cited reference.

Independent claim 10 is allowable over the cited references in that it recites a combination of elements including, for example "a seal pattern of constant thickness formed between the upper substrate and the lower substrate along a boundary region between the display area and the non-display area, the seal pattern having an injection hole and contacting the gate insulating layer".

The structure of claim 10 of the present invention is different from the structures in the cited references in that none of the references disclose "a seal pattern of constant thickness formed between the upper substrate and the lower substrate along a boundary region between the display area and the non-display area, the seal pattern having an injection hole and contacting the gate insulating layer". The Examiner acknowledges that Fujioka '764 does not disclose or

suggest that the seal pattern contacts the gate insulating layer (Office Action, page 7). However, as discussed above, Fujioka '439 also does not disclose or suggest this feature. Fig. 20 of Fujioka '439 clearly shoes that the sealing material 28 contacts both the insulating material 50 and the gate insulating layer 38 at different heights making the thickness of the sealing material variable.

Fujioka '439 discloses that "the sealing material 28 can be directly contacted with the gate insulating film 38 of the substrate 22 and the light-shading layer (a black matrix made from a metal such as Cr) of the substrate 24 in the adhesion reinforcing portion 50a" (Fujioka '439, column 18, lines 50-54). Therefore, Fujioka '439 does not disclose or suggest "a seal pattern of constant thickness formed between the upper substrate and the lower substrate" as recited in claim 10.

The Examiner implicitly acknowledges that none of Sakamoto, Obara or the other cited references disclose or suggest this feature. Accordingly, claim 10 and claim 11 which depend from claim 10 are allowable over the cited reference.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at (202) 496-7500 to discuss the steps necessary for placing the application in condition for allowance. All correspondence should continue to be sent to the below-listed address.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911. A duplicate copy of this sheet is enclosed.

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Respectfully submitted,

By _____

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